Electronic Devices, Vol. 36, No. 11, (Nov. 1989)) in the Final Office Action dated August 1, 2001. This rejection is respectfully traversed.

Doyle

It is the Examiner's position that Doyle et al. discloses essentially each and every step of the method recited in independent claim 1, except that the reference fails to show use of a refractory metal for the recited depositing step. To cure this deficiency in the reference, the Examiner takes official notice that it is well known in the art to use cobalt as a refractory metal for its low resistance, and because it forms a stable silicide with polysilicon.

In a response dated June 5, 2001, the applicants pointed out functional and structural differences between the reference and the Applicants' claimed invention, notwithstanding the Examiner's official notice. In the present Office action (page 7) the Examiner responded to the Applicants' Remarks, and concluded that they have been fully considered, but are not persuasive.

The Applicants asserted, and now reassert (with pinpoint citations) that not only Doyle, but Broadbent (the other applied reference) include the step ***of siliciding the gate electrode prior to depositing a metal layer***. As the Applicants previously stated, one of the novel aspects of the Applicants' claimed method is that a separate silicide processing step (siliciding of the gate)

is avoided by depositing a metal layer directly on a polysilicon layer in forming the silicide layer.

In the Office Action dated August 2, 2001, the Examiner asserts that the gate silicide 110 of Doyle is removed by CMP prior to depositing the refractory metal (col. 3, lines 13-14). This is not so; neither is it necessary to make an analysis that goes beyond the plain language of Doyle to see that gate silicide 110 is not removed during the CMP polishing step.

The discussion related to the removal of the sacrificial layer by CMP begins at col. 3, line 10 and progresses to lines 13-14 (cited by the Examiner), and is quoted as follows:

> As shown in FIG. 1(c), sacrificial dielectric layer 114 is then processed to remove an uppermost portion in order to expose the top surface of the gate electrode. Typically, the top portion of sacrificial layer 114 is removed by chemical mechanical polishing (CMP).
>
> Doyle, col. 3, lines 10-14

The above quote yields at least two facts that are relative to the Applicants' position. First, only the sacrificial dielectric layer is removed (not silicide layer 110) by CMP. Second, we are directed to figure 1(c) for an illustration of the result of the described CMP step. Looking to figure 1(c) then, as directed, we see that ***silicide layer 110 is still intact after the CMP polishing step***.

The Examiner continues this line of reasoning by referring to the disclosure of Doyle in column 3, lines 60-63 that formation of source and drain

silicide is not a requirement of the invention, and also Doyle column 2, lines 53-55 i.e., source/drain silicide layer 112 and gate silicide 110 are formed concurrently.

In other words, according to the Examiner, since source/drain regions are silicided concurrently with the gate layer, and since formation of source and drain silicides is not a requirement of their invention, then it must also be true that formation of a gate silicide is also not a requirement of the invention. Such a conclusion is unreasonable. If the requirement of the source/drain silicide is retracted, it would have been fairly simple, if intended, to retract the requirement of the gate silicide. Doyle did not do so; therefore it is unfair to conclude that it was Doyle's intention to retract the requirement of siliciding the polysilicon gate prior to depositing a metal layer.

Applicants' point is repeatedly reinforced by the claim language in Doyle, column 4.The Line 14 recites "reacting the conductive material to form silicided source and drain regions, and a ***silicide layer having a first thickness on the gate electrode***;" line 18 recites "removing an uppermost portion of the sacrificial layer ***until the silicide layer is exposed***;" line 21 recites "depositing a second conductive material ***over both the sacrificial layer and the silicide layer***;" line 22 recites "*forming a silicide layer having a second thickness*" (emphasis added).

Therefore, the lack of a requirement to form silicide source/drain regions does not implicitly translate into the lack of a requirement to form silicide layer

110. Accordingly, Doyle does not disclose or suggest forming a first insulating film and a non-silicide conductive film on a semiconductor substrate or depositing a refractory metal layer on an entire surface such that the refractory metal layer is adjacent to the patterned conductive film as recited in independent claim 1 and similarly stated in independent claim 10.

Broadbent

Similarly, Broadbent fails to anticipate the novel aspects of the Applicants' claimed method. Broadbent, like Doyle, forms a gate silicide prior to depositing a metal directly on the gate for forming another gate silicide. In fact, Broadbent describes this process as typical, further amplifying the novelty of the Applicants' method of avoiding the additional gate siliciding process.

Particularly, Broadbent, page 2441, beginning at line 8, discloses a separate silicide processing step for source/drain, and polycrystalline Si ***gate regions*** by ***using a silicide, $TiSi_2$***, to reduce sheet resistivity. Therefore while it may be true that the use of cobalt forms a stable silicide with polysilicon (as the Examiner claims), it is not disclosed in Broadbent. At least, because of the intervening formation of ***$TiSi_2$*** on the gate prior to depositing a metal layer, Broadbent does not disclose or suggest forming a first insulating film and a non-silicide conductive film on a semiconductor substrate or depositing a refractory metal layer on an entire surface such that the refractory metal layer

is adjacent to the patterned conductive film as recited in independent claim 1 and similarly stated in independent claim 10.

Since neither Doyle, nor Broadbent disclose or suggest the features of independent claims 1 and 10, claims 2-9 and 12-21, dependent on claims 1 and 10, are not rendered obvious to one of ordinary skill in the art. Reconsideration and withdrawal of this art grounds of rejection is respectfully requested.

Rejections Under 35 U.S.C. § 102

The Examiner rejected claim 22 (now claim 21) under 35 U.S.C §102(e) over U.S. Patent No. 6,025,254 to Doyle et al. (Doyle). Applicants respectfully traverse the rejection.

Doyle (argued above) does not disclose forming a first insulating film and a non-silicide conductive film on a semiconductor substrate or depositing a refractory metal layer on an entire surface such that the refractory metal layer is adjacent to the patterned conductive film as recited in independent claim 1 and similarly stated in independent claim 10.

Doyle discloses that:

> As shown in FIG. 1(c), sacrificial dielectric layer 114 is then processed to remove an uppermost portion in order to expose the top surface of the gate electrode. Typically, the top portion of sacrificial layer 114 is removed by chemical mechanical polishing (CMP). It will be appreciated by those skilled in the art having the

benefit of this disclosure that **the top portion of a sacrificial layer may also be etched back**.

Doyle, col. 3, lines 10-16 (emphasis added)

It is shown in figures 1(b) and 1(c) of Doyle that a portion of silicide layer 110 is removed, and further in the above quote from Doyle that etching may be employed instead of CMP. Besides, etching the silicide layer is within the purview of those of ordinary skill in the art (according to Doyle).

Therefore Doyle does not teach forming a silicide pattern on the gate insulating layer without etching the silicide from which the silicide pattern is fabricated as recited in claim 22 (now claim 21). Accordingly, reconsideration and withdrawal of this art grounds of rejection is respectfully requested.

CONCLUSION

Applicants point out that all of the Examiner's comments have been addressed and that all of the Examiner's objections and rejections have been overcome, thereby placing all claims pending in the present Application in condition for allowance. Allowance of the claims is respectfully solicited.

In the event that any outstanding matters remain in this application, Applicant requests that the Examiner contact the undersigned at (703) 205-8000 to discuss such matters.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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